MUHAMMAD HAMZA MUNEER

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EXPERIENCE

10 JULY 2017 – TILL DATE

SENIOR EMBEDDED SYSTEM ENGINEER, POWERSOFT19 (PAKISTAN)

As a Senior Embedded System Engineer with seven years of experience, I develop embedded systems on platforms like processors, SoCs, CPLDs, and FPGAs. My expertise includes driver development, application programming, and software architecture design.

I perform FMECA, FMEA, and implement FRACAS to manage system failures. I collaborate with hardware and production teams for product optimization and lead a team designing SIL-3 safety-critical systems using the OODA loop.

I have deep knowledge of ARM Cortex, Xilinx, and Altera architectures, and experience with EV charging standards like OCPP, OCPI, ISO 15118, CCS, and CHAdeMO. I also excel in working with offshore teams.

My job duties include:

- Planning project, allocating resources and holding regular meetings with the team
- Driver development e.g., Ethernet, PCIe, MII, SDIO, CAN, UART, SPI, I2C etc.
- Development of controls and communication using MCUs, FPGAs and SOCs
- Coordination with teams for in house testing, prototype and system verification
- Providing Support for Field Deployments and commissioning
- Supervising junior engineers and ensuring timely delivery of the software

FPGA / CPLD Development

- Deep understanding of Xilinx FPGAs and Zynq 7000 SOC architecture.
- Implemented FOTA (Firmware Over-The-Air) and Partial Reconfiguration for FPGAs
- Design and Implementation of custom synchronous / asynchronous serial protocol.
- Implemented High Speed Distributed Controls for L3 EV DC Fast Chargers
- Implementation of control from bi-directional DAB.
- Implemented Time Syncing between different boards at the resolution of 100 ns.
- Driver development for high-speed ADC and DACs for control of grid-tied inverters
- Driver development of Gigabit Ethernet, in both FPGA and processor
- Worked on the development of communication based on PCIe using Zynq devices.
- Implementation of DSP algorithms on FPGAs and SOCs

Microprocessor Development

- Porting CANopen stack on ARM Cortex A9
- Implementation of wear-leveling algorithm on Infineon processors
- RTOS porting and development on Zynq 7000 series SOCs
- Integration of TLS over TCP/IP (lwIP) on ARM Cortex M4 (STM32)
- HMAC design & implementation for low memory embedded systems
- Development of FDR (Fault Data Recorder) for logging events (Resolution up to 100 ns)
- Development of a time syncing routine at microseconds level for a cyber-physical system
- Custom Bootloader development for ARM Processors.
- Implemented FOTA (Firmware Over-The-Air) on Xilinx, ARM (NXP, STM32, Nordic).
- Hands on experience of multicore processing in ARM, Xilinx, and Infineon processors.
- Good understanding of PetaLinux and Yocto Project for Linux.

01 JUNE 2022 – 31 DECEMBER 2023

SENIOR EMBEDDED SUPPORT ENGINEER, ACESO ANALYTICS (UNITED KINGDOM) - REMOTE

My main responsibilities include working with the team for

- Embedded architecture selection and design
- Code Reviews & debugging

EDUCATION

MS ELECTRICAL ENGINEERING, LAHORE UNIVERSITY OF MANAGEMENT SCIENCES (LUMS) LAHORE – OCTOBER 2020

Majors: Embedded Systems | CGPA: 3.2

BS ELECTRICAL ENGINEERING, UNIVERSITY OF ENGINEERING & TECHNOLOGY (UET) LAHORE – JULY 2017

Majors: Computer Systems | CGPA: 3.1

JOURNAL PUBLICATION

AUGUST 2023 | IMPACT FACTOR: 4.3

M. H. Muneer, M. A. Pasha, and I. R. Khan, **"Hardware-friendly tone-mapping operator design and implementation for real-time embedded vision applications,"** Computers and Electrical Engineering, vol. 110, p. 108892, 2023.

SKILLS

PROCESSORS, CONTROLLERS, FPGA, SOCS, CPLDS

ARM Cortex-M| ARM Cortex-A | Infineon Tri-core | Xilinx Zynq Ultrascale+ | Xilinx Zynq 7000 | Xilinx 7 Series FPGAs | Altera Cyclone III SOC | Altera Max V CPLDs

IDES, COMPILERS, SYNTHESIZERS, SIMULATORS, DEBUGGERS

Keil | IAR | Eclipse | Codeblocks | Cadence Virtuoso, NCSim, Genus, Innovus | Xilinx Vivado, ISE | Quartus Prime | Modelsim | Jlink | ST-Link

PROGRAMMING CAPABILITIES

C | Embedded C | VHDL | Verilog | RTOS | C++ | Linux

TOOLS AND TECHNIQUES

JIRA | Polarion | Git | SVN | Agile | SCRUM

MASTER'S THESIS

HARDWARE FRIENDLY AND RESOURCE EFFICIENT TONE MAPPING OPERATOR

Design and CPU, FPGA and GPU Implementation of propriety hardware friendly and resource efficient tone mapping operator from tone mapping HDR images to LDR images.

PROJECTS

COMPUTER VISION BASED TACTICAL COMBAT ROBOT

Use of embedded Linux for development of computer vision based tactical combat robot equipped with point and shoot algorithm and facial recognition algorithms.

DESIGN AND IMPLEMENTATION OF A CUSTOM REAL-TIME OPERATING SYSTEM (RTOS)

Development of a custom RTOS which includes Round-Robin and Periodic schedulers.

FPGA IMPLEMENTATION OF A-SYMMETRIC ENCRYPTION/DECRYPTION ALGORITHM

Implementation of Elliptic Curve Cryptography (ECC) on Altera Cyclone-V FPGA board

ASIC IMPLEMENTATION OF TONE MAPPING OPERATORS

Implemented tone mapping operators using Cadence Genus and Innovus on 180nm technology.